IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Joy, William; Tremblay, Marc		
Assignee:	Sun Microsystems, Inc.		
Title:	Efficient Handling Of A Large Register File For Context Switching		
Serial No.:	Not yet assigned	Filing Date:	Herewith
Examiner:	Eng., D.	Group Art Unit:	2155
Docket No.:	SP-2612-1C US		

Newport Beach, California
March 19, 2001

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PRELIMINARY AMENDMENT

Dear Sir:

The following Amendments and Remarks are submitted for entry into the above-named application. Please enter the following amendments.

AMENDMENTS

Please amend the above-referenced application as follows:

In the Specification

Kindly delete the cross-reference table from Pages 29-30.

On Page 1, on the first line of the specification, kindly insert, as follows:

Cross-Reference

The present application is a continuation of United States patent no. 6,205,543 entitled, "Efficient Handling of a Large Register File for Context Switching", naming Marc Tremblay and William Joy as inventors and issued on March 20, 2001.

The present invention is related to subject matter disclosed in the following co-pending patent applications:

1. United States patent application serial no. 09/204,480 entitled, "A Multiple-Thread Processor for Threaded Software Applications", naming Marc Tremblay and William Joy as inventors and filed on December 3, 1998;

2. United States patent application serial no. 09/204,584 entitled, "Clustered Architecture in a VLIW Processor", naming Marc Tremblay and William Joy as inventors and filed on December 3, 1998;

3. United States patent application serial no. 09/204,481 entitled, "Apparatus and Method for Optimizing Die Utilization and Speed Performance by Register File Splitting", naming Marc Tremblay and William Joy as inventors and filed on December 3, 1998;

4. United States patent application serial no. 09/204,536 entitled, "Variable Issue-Width VLIW Processor", naming Marc Tremblay as inventor and filed on December 3, 1998;

5. United States patent application serial no. 09/205,121 entitled, "Dual In-line Buffers for an Instruction Fetch Unit", naming Marc Tremblay and Graham Murphy as inventors and filed on December 3, 1998;

6. United States patent application serial no. 09/204,781 entitled, "An Instruction Fetch Unit Aligner", naming Marc Tremblay and Graham Murphy as inventors and filed on December 3, 1998;

7. United States patent application serial no. 09/204,535 entitled, "Local Stall Control Method and Structure in a Microprocessor," naming Marc Tremblay and Sharada Yeluri as inventors and filed on December 3, 1998;

8. United States patent application serial no. 09/204,585 entitled, "Local and Global Register Partitioning in a VLIW Processor", naming Marc Tremblay and William Joy as inventors and filed on December 3, 1998; and

9. United States patent application serial no. 09/204,479 entitled, "Implicitly Derived Register Specifiers in a Processor", naming Marc Tremblay and William Joy as inventors and filed on December 3, 1998.

In the Drawings

Kindly replace the original drawings with the attached formal drawings.

In the Claims

Kindly cancel all claims in the parent application and add new claims 1-5, as follows:

1. A context switch controller in a processor that includes an operand data storage for holding data operated upon by instructions executing on the processor, the operand data storage being divided into a plurality of storage groups containing one or more storage elements, the context switch controller comprising:

a dirty bit storage including one or more storage bits that correspond to one or more respective storage groups in the operand data storage; and

a dirty bit logic coupled to the dirty bit storage and coupled to receive a destination address field of the instructions, the dirty bit logic responsive to an executed instruction by classifying a destination access as a targeted storage group according to information in the destination address field of the executed instruction and by evaluating the classified destination based on whether the instruction updates the targeted storage group.

2. A context switch controller according to Claim 1 wherein:

the dirty bit logic is responsive to a context switch by saving storage groups based on the evaluation of the classified destinations.

3. A processor comprising:

a plurality of functional units;

a register file including a plurality of register file segments coupled to and associated with the plurality of functional units, respectively, the register file being divided into a plurality of register groups;

a dirty bit register coupled to the register file; and

means coupled to the dirty bit register for accessing a destination register (rd) field of an instruction;

means for classifying the destination register rd according to the address in the rd field, the classification corresponding to a bit in the dirty bit register; and

means for evaluating the dirty bit register to designate that the particular classification includes a register that is written by the instruction.

4. A processor according to Claim 3 further comprising:

means coupled to the dirty bit register and coupled to the register file for storing a plurality of dirty bits designating enablement or disablement of access to the register file on a register group-by-register group basis; and

means responsive to an instruction that accesses the register file for determining whether access is enabled by the dirty bit of the dirty bit enable register corresponding to the register group of the register file accessed by the instruction, permitting access if access is enabled.

5. A context switching logic in a processor that includes an executive storage for holding operand data operated upon by instructions executing on the processor, the executive storage being divided into a plurality of storage groups containing one or more storage elements, the context switching logic comprising:

means for utilizing a dirty bit storage including a plurality of storage bits corresponding to a plurality of respective storage groups in the executive storage;

means for receiving a destination address field of the executing instructions;

means for responsive to an executed instruction, classifying a destination access as a targeted storage group according to information in the destination address field of the executed instruction;

means for evaluating the classified destination based on whether the instruction updates the targeted storage group; and

13 means responsive to a context switch for saving storage groups based on the evaluation of the
14 classified destinations.

REMARKS

The specification is amended to update the cross-reference table, submit formal drawings, remove allowed claims of the parent application, and add new claims.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to telephone the undersigned at (949) 718-5200.

EXPRESS MAIL LABEL NO:

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Respectfully submitted,

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